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68231 U.S. PTO
08/18/97

CERTIFICATE OF EXPRESS MAILING

I hereby certify that this 37 CFR §1.60 request and the documents referred to as attached therein are being deposited with the United States Postal Service on in an envelope as "Express Mail Post Office to Addressee" service under 37 CFR §1.10, Mailing Label Number **EM533238587US** addressed to the Commissioner of Patents and Trademarks, Washington, DC 20231.

Date: August 18, 1997

Kimberly Lane

Docket No. CDT001A
Anticipated Classification of this Application:
Class: Subclass:
Prior Application Serial No.: 08/262,754
Examiner: Heckler, T.
Art Unit: 2316

4881990*65247680

CONTINUATION / DIVISIONAL APPLICATION UNDER 37 C.F.R. § 1.60

(May not be used for a continuation-in-part application, 37 C.F.R. § 1.53, M.P.E.P. § 201.06(a))

Commissioner of Patents and Trademarks
Washington, DC 20231

Sir:

This is a request for filing a

☒ Continuation ☐ Divisional

application under 37 C.F.R. § 1.60 of pending prior application U.S. Serial No. 08/262,754 filed on June 20, 1994 in the name of C. Douglass Thomas et al., and from which priority under 35 U.S.C. § 120 is claimed.

Enclosed is a True Copy of the Prior Complete Application as Filed including:

- ☒ 24 page(s) of Specification and Claims,
- ☒ 1 page of Abstract,
- ☒ 7 sheet(s) of Drawings,
- ☒ 1 pages Combined Declaration and Power of Attorney,
- ☐ __ pages of an Amendment referred to in the Declaration filed to complete the Prior Application.

Also Enclosed:

- ☐ An Information Disclosure Statement.
- ☒ A Verified Statement that this filing is by a small entity:
  - ☐ is attached.
  - ☒ was filed in a parent application; such status is still proper and desired (37 CFR §1.28(a)). Copy enclosed.
- ☒ New formal drawings (8 sheets).
- ☐ There is provided herewith a Petition to Suspend Prosecution for the Time Necessary to File an Amendment (New Application Filed Concurrently).

Assignment

☐ The prior application is assigned of record to

_____

☐ An assignment of the invention to _____ is attached. An Assignment Recordation Cover Sheet for recordation of the assignment is also submitted herewith.

Extension of Time for Prior Pending Application

☐ A Petition for Extension of Time is being concurrently filed in the prior pending application. A copy of the Petition for Extension of Time in the prior pending application is attached.

☐ A Conditional Petition for Extension of Time is being concurrently filed in the prior pending application. A copy of the Conditional Petition for Extension of Time in the prior pending application is attached.

Claim For Foreign Priority

☐ Priority of _____ Application No. _____ filed on _____ is claimed under 35 U.S.C. § 119.

☐ The certified copy has been filed in prior pending application U.S. Serial No. _____

☐ The certified copy will follow.

Amendments

☐ Cancel in this application original claim ___ of the prior application before calculating the filing fee. (*At least one original independent claim must be retained for filing purposes.*)

☐ A preliminary amendment is enclosed. *(New claims are numbered consecutively after the highest original claim in the prior application.)*

☒ Amend the specification by inserting before the first line the sentence:

"This is a

☒ Continuation ☐ Divisional

application of copending prior

☒ application Serial No. 08/262,754 filed on 6/20/94,

☐ International Application _____ filed on _____ which designated the United States,

the disclosure of which is incorporated herein by reference."

Inventorship:

With respect to the prior copending U.S. Application from which this application claims benefit under 35 USC §120, the inventor(s) in this application is (are):

☒ the same.

☐ less than those named in the prior application and it is requested that the following inventor(s) identified above for the prior application be deleted:

_____.

Fee Calculation (37 CFR § 1.16)

	(Col. 1) NO. FILED	(Col. 2) NO. EXTRA	SMALL ENTITY RATE	FEE	OR	LARGE ENTITY RATE	FEE
BASIC FEE			$385	$	OR	$770	$
TOTAL CLAIMS	20	-20 = 0	x11 =	$ 0	OR	x22 =	$
INDEP CLAIMS	3	-03 = 0	x40 =	$ 0	OR	x80 =	$
[ ] Multiple Dependent Claim Presented			130 =	$	OR	260 =	$
* If the difference in Col. 1 is less than zero, enter "0" in Col. 2.			Total	$ 385	OR	Total	$

☒ Our Check No. 207802 in the amount of $ 385.00 for basic filing and claim fees and any assignment recordation fee is enclosed.

Power of Attorney

☒ The Power of Attorney appears in the prior application and is effective for this application.

OR

☐ A New or Associate Power of Attorney is enclosed.

☐ Address all future communications to:

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METHOD AND SYSTEM FOR CONTROLLING A PROCESSOR'S CLOCK FREQUENCY IN ACCORDANCE WITH THE PROCESSOR'S TEMPERATURE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a computing device and, more particularly, to a method and apparatus for controlling a processor's clock frequency.

2. Description of the Related Art

It is known that if no user activity has occurred for a period of time that a portable computer can be placed in a suspend or sleep mode. It is also known to suspend or slow a computer's processor (e.g., microprocessor, CPU) when the processor is not actively processing. The following patents and patent publications are representative of the current state of the art:

(a) U.S. Patent 5,201,059 discloses a sleep mode which is activated when control given to BIOS or alternatively by incorporating some statistical analysis of the frequency of BIOS calls. In this patent, the sleep mode either stops the clock or slows it to 4 MHz.

(b) U.S. Patent 5,167,024 discloses a power management system for a laptop computer. The power management system operates to disconnect power sources and/or clock signals to various peripheral devices to conserve battery power. The slow mode is entered into when no activity has been detected for a predetermined period of time.

(c) U.S. Patent 5,218,704 discloses a technique for power conservation based on real-time sampling of CPU activity. The activity is sampled during interrupts and when it determines that the CPU may rest, a sleep clock is

supplied to the CPU. The detection of an interrupt restores the clock to the fast rate prior to processing the interrupt.

(d) U.S. Patent 5,239,652 discloses a technique for power consumption which disconnects the CPU from the power supply when control logic determines the CPU is not actively processing. Thereafter, the CPU is periodically powered-up to perform housekeeping chores as well as to determine it normal processing should be resumed.

(e) European patent publication EP-0474963 discloses a sleep mode controller which lowers the CPU clock speed when no input/output operation (when keyboard control routine of BIOS executed no input key data in key buffer, or when CPU is idle and no input key data in the key buffer) is performed. The system uses a clock generator circuit which produces the low clock (4 MHz), the high clock (32 MHz) and a slightly slower high clock (16 MHz). A keyboard controller is used to determine which of the high clocks is used, with selection being made by the computer user. The sleep mode controller is disabled if the AC adapter is connected.

(f) U.S. Patent 5,230,055 discloses a portable computer wherein the computer is make inoperable when ambient temperature or humidity become too high. Here, ambient temperature and humidity are periodically monitored.

(g) European patent publication EP-0381021 discloses a power saving system for a personal computer. The system operates to allow or stop power to be supplied to an oscillator based on control data set to a control register via keyboard or software.

(h) U.S. Patent 5,021,679 discloses a power system for a portable computer wherein the supply voltage is varied depending on the current being supplied to the computer by the power system. Further, a variable-frequency

clock is provided which varies its frequency based on the supply voltage being produced.

External clocks have been used to provide a computer system with faster clocks. Here, the faster external clock is substituted for the internal clock of the computer system. U.S. Patent 5,134,703 is illustrative of an external clock unit which supplies a faster clock to a computer without requiring any hardware changes within the computer.

The problem with all the prior solutions to energy conservation is that the processors can still overheat. In particular, during prolonged processing or activity by a computer's processor, the processor will not enter its sleep mode (if any) and as a result the processor will become hot and require extensive means to cool the processor to prevent overheating and eventual failure of the processor. Overheating and failure of the processor can also occur when the computer is used in particularly hot environmental temperatures, the computer's cooling fan fails, or when cooling of the processor is otherwise inadequate.

Another problem is that with portable computers, manufacturers have to either use a lower clock frequency (lower than would be used in a comparable desk top computer) for processing or provide a fan for cooling. A lower clock frequency is not satisfactory as users want maximum processing power just as they get with a desk top computer. Requiring a portable computer to use a fan for cooling is also unsatisfactory because it consumes battery energy.

Thus, there is a need for a solution to the above problems which enables a computing device to maximize its processing speed while, at the same time, preventing overheating.

SUMMARY OF THE INVENTION

Broadly speaking, the invention relates to novel techniques for controlling a processor's clock frequency so as to prevent overheating. While preventing overheating, the invention attempts to maximizes the processing speed of the processor.

The invention monitors a processor's activity and its temperature. When there is no activity for the processor, a slowed clock frequency is used, thereby saving power and lowering the thermal heat produced by the processor. On the other hand, when there is activity for the processor, a fast clock frequency is used. However, when prolonged activity (i.e., sustained fast clock frequency) causes the processor's temperature to become dangerously high for proper operation, the clock frequency is reduced so as to maintain processing speed at a reduced speed while preventing overheating. The invention may be implemented as an apparatus or a method.

As an apparatus, the invention can be implemented as a computer which includes: a clock module for producing a clock signal having two or more different frequencies; a processor for processing instructions in accordance with the clock signal; and a temperature sensor producing a temperature signal based on the temperature of the processor. In accordance with the invention, the frequency of the clock signal supplied to the processor is varied depending on the temperature of the processor. Preferably, the processor is a microprocessor.

As a method, the invention produces a clock for a microprocessor. The method includes monitoring chip temperature of the microprocessor, producing a clock signal having a frequency which varies in accordance with the chip temperature, and supplying the clock signal to the microprocessor. Specifically, when the chip temperature exceeds a predetermined temperature,

the frequency of the clock signal is slowed. The method may also monitor activity of the microprocessor so that a slowed frequency clock is produced when there is no activity at the microprocessor. Several enhancements to this basic implementation are also described and claimed, including the use of an overdrive clock.

Other aspects and advantages of the invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principals of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be readily understood by the following detailed description in conjunction with the accompanying drawings, wherein like reference numerals designate like structural elements, and in which:

FIG. 1 is a block diagram of a first embodiment of the invention;

FIG. 2 is a graph of an example of the relationship of chip temperature of a microprocessor and frequency of a clock signal;

FIG. 3 is a block diagram of a second embodiment of the invention;

FIG. 4 is a block diagram of a third embodiment of the invention;

FIG. 5 is a block diagram of a fourth embodiment of the invention;

FIG. 6 is a timing diagram illustrating operation of the fourth embodiment;

FIG. 7 is a block diagram of a fifth embodiment of the invention;

FIG. 8 illustrates a schematic diagram of an embodiment of an activity detector;

FIG. 9 is a block diagram of a sixth embodiment of the invention; and

FIG. 10 is a block diagram of a seventh embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

The invention provides novel techniques for controlling a processor's clock frequency so as to prevent overheating. In addition to preventing overheating, the invention attempts to maximize the processing speed of the processor. The invention also operates to conserve the amount of energy consumed by the processor. Preventing the processor from overheating is important because when a processor overheats it no longer operates properly. Conservation of energy, although of general importance for all computing devices, is particularly important for portable computing devices.

The invention monitors a processor's activity and its temperature. When there is no activity for the processor, a slow clock frequency is used, thereby saving power and lowering the thermal heat produced by the processor. On the other hand, when there is activity for the processor, a fast clock frequency is used. However, when prolonged activity (i.e., sustained fast clock frequency) causes the processor's temperature to become dangerously high for proper operation, the clock frequency is reduced so as to maintain processing speed at a reduced speed while preventing overheating.

Embodiments of the invention are discussed below with reference to figures 1-10. However, those skilled in the art will readily appreciate that the detailed description given herein with respect to these figures is for explanatory purposes as the invention extends beyond these limited embodiments.

FIG. 1 is a block diagram of a first embodiment of the invention. In this embodiment, a microprocessor 2 has a temperature sensor 4 which is integral with the microprocessor 2. The temperature sensor 4 is either integrated within the Very Large Scale Integration (VLSI) design of the microprocessor 2 or placed in contact with the housing or package thereof. In either case, the temperature sensor 4 is thermally coupled with the microprocessor 2. Because

the temperature sensor 4 is integral or thermally coupled with the microprocessor 2, the temperature sensor 4 is very responsive to the temperature changes of the microprocessor 2. The temperature sensor 4 produces a temperature signal 6. Temperature sensing circuitry is well known and therefore not further described.

The temperature signal 6 is supplied to a voltage-controlled oscillator (VCO) 8. The VCO 8 produces a clock signal 10 which is supplied to a clock input of the microprocessor 2. The VCO 8 operates to produce different frequencies for the clock signal 10 depending on the value of the temperature signal. In this embodiment, the temperature signal 6 is preferably an analog voltage signal and the VCO 8 produces the clock signal 10 based on the value of the analog voltage signal. For example, the temperature signal could be a voltage ranging from zero to five volts. In response to the temperature signal 6, the VCO 8 could produce the clock signal with frequencies ranging from 100 MHz to 1 MHz. The frequency range is a design choice selected in accordance with the specific microprocessor being utilized. VCO's are well known and therefore are not further described.

FIG. 2 is a graph of an example of the relationship of chip temperature of the microprocessor 2 and clock frequency of the clock signal 10. The clock frequency varies between a maximum frequency (fMAX) and a minimum frequency (fMIN) for given microprocessor. The minimum frequency (fMIN) may be zero if the clock signal 10 is not responsible for refreshing dynamic memory; otherwise, it cannot fall below some minimum frequency. Notice that as the chip temperature increases beyond some threshold temperature (VTH) (e.g., 120 degrees F), the frequency of the clock signal 10 will gradually decrease. By decreasing the clock frequency in relation to the chip temperature, processing speed can be maximized for a given temperature

without risking processor overheating. As the chip temperature become "hot", the clock frequency is reduced so as to reduce the thermal heat generated by the microprocessor 2. The profile of the curve for the clock frequency shown in FIG. 2 is illustrative as other curves may be used. For example, the frequency of the clock signal 10 could be controlled so that the chip temperature is maintained in a more limited temperature range. In any case, the profiles of the curves decrease the clock frequency as the temperature increases.

FIG. 3 is a block diagram of a second embodiment of the invention. In this embodiment, the microprocessor 2, temperature sensor 4, the temperature signal 6, the VCO 8, and the clock signal 10 are similar to those utilized in the first embodiment. However, this embodiment further includes an activity detector 12, an activity signal 14, a VCO controller 16, and a control signal 18.

The activity detector 12 monitors the microprocessor 2 and/or some related peripheral device (e.g., interrupt controller, keyboard buffer, input/output ports, instruction cache, current instruction, program counter) to determine when the microprocessor 2 is actively processing or when processing is needed. In this case, the activity detector 12 notifies the VCO controller 16 that processing is needed with the activity signal 14. On the other hand, when no activity exists, the activity detector 12 notifies the VCO controller 16 that no processing is needed with the activity signal 14. The activity signal is preferably a digital signal having at least one bit. Activity detection is described in more detail in U.S. Patent 5,201,059; U.S. Patent 5,167,024; U.S. Patent 5,218,704; U.S. Patent 5,239,652; and European patent publication EP-0474963, which are hereby incorporated by reference.

The VCO controller 16 receives the activity signal 14 and the temperature signal 6. In response to these signals, the VCO controller 16 produces the control signal 18 which controls the VCO 8. The control signal

18 may be analog or digital depending on the design of the VCO 8. The basic operation of the VCO controller 16 is to cause the VCO 8 to produce the clock signal 10 for the microprocessor 2 in an intelligent manner so as to conserve energy and prevent overheating. Namely, if the activity detector 12 indicates that no processing is needed at a given point in time, then regardless of the temperature detected by the temperature sensor 4, the VCO controller 16 will cause the VCO 8 to produce a sleep (or slow) clock. The sleep clock has a frequency near the minimum frequency (fMIN). On the other hand, if the activity detector 12 indicates that processing is needed at this point in time, then the VCO controller 16 will cause the VCO 8 to produce a fast clock. The fast clock is the temperature-regulated maximum frequency such as discussed in FIGS. 1 and 2.

The second embodiment is particularly advantageous for portable computing devices because it conserves battery life by using a sleep clock when no processing is needed. However, even in the case of prolonged processing, the embodiment prevents overheating.

FIG. 4 is a block diagram of a third embodiment of the invention. In this embodiment, the microprocessor 2 includes a clock regulation unit 20 which controls the frequency of the clock used by the microprocessor 2 based on chip temperature of the microprocessor 2. Preferably, the clock regulation unit 20 is integrated with circuitry of the microprocessor 2. Alternatively, the clock regulation unit 20 can be separate from the circuitry of the microprocessor 2 but nevertheless coupled thereto.

The clock regulation unit 20 receives an input clock from an oscillator 22 and produces an output clock which is used by the microprocessor 2. The clock regulation unit 20 includes a temperature sensor 4, a divider 24, a first AND gate 26, a second AND gate 28, an inverter 30 and an OR gate 32. The

temperature sensor 4 is as previously described. The divider 24 divides the input clock (fast clock) from the oscillator 22 to produce a sleep (or slow) clock. For example, if the oscillator 22 is a 100 MHz fixed-frequency oscillator and the divider 24 divides by 100, then the sleep clock would be 1 MHz.

In this embodiment, the temperature sensor 4 produces a digital output. It is assumed that the digital output is normally "0", but when the microprocessor 2 becomes "hot", the digital output becomes "1". The digital output of the temperature sensor 4 together with the logic gates 26-32 operate to select either the fast clock or the sleep clock as the output clock which is used by the microprocessor 2. In particular, when the microprocessor 2 is not "hot", AND gate 26 is inactivated and AND gate 28 is activated by inverter 30. Hence, the output clock is the fast clock via AND gate 28 and OR gate 32. On the other hand, when the microprocessor 2 is "hot", AND gate 26 is activated and AND gate 28 is inactivated. Accordingly, in this case, the output clock is the sleep (or slow) clock via AND gate 26 and OR gate 32. FIG. 5 is a block diagram of a fourth embodiment of the invention. In this embodiment, the microprocessor 2 includes a clock regulation unit 20 which controls the frequency of the clock used by the microprocessor 2 based on chip temperature of the microprocessor 2 and processing activity. The clock regulation unit 20 is preferably integrated with circuitry of the microprocessor 2.

As with the third embodiment, the clock regulation unit 20 for the fourth embodiment receives the input clock from the oscillator 22 and produces the output clock which is used by the microprocessor 2. The clock regulation unit 20 includes the temperature sensor 4, the divider 24, the first AND gate 26, the second AND gate 28, and the OR gate 32 as described above with reference to FIG. 4. The divider 24 divides the input clock (fast clock) from the oscillator

22 to produce a sleep clock. The temperature sensor 4 produces a digital output. Although the digital output from the temperature sensor 4 is normally "0", when the microprocessor 2 becomes "hot", the digital output becomes "1". The activity detector 12 produces an activity signal as described in the second embodiment. Here, the activity signal is a digital signal which is "high" or "1" when activity is present and "low" or "0" when no activity is present.

The digital output of the temperature sensor 4 together with the activity signal from the activity detector 12 and the logic gates 26, 28, 32, 34, 36 and 38 operate to select either the fast clock or the sleep clock. In particular, when the microprocessor 2 is not "hot" and activity is present, the AND gate 36 is activated by the inverter 34 and the activity signal. The output of AND gate 36 then activates AND gate 28 and inverter 38 inactivates AND gate 26. Hence, the output clock is the fast clock via AND gate 28 and OR gate 32. On the other hand, when the microprocessor 2 is "hot", the AND gate 36 is inactivated by the inverter 34 regardless of the activity signal. The output of AND gate 36 inactivates AND gate 28, and inverter 38 activates the AND gate 26. In this case, the output clock is the sleep clock via AND gate 26 and OR gate 32.

FIG. 6 is a timing diagram illustrating operation of the fourth embodiment. The output clock (CLK) is a mixture of the fast clock produced by the oscillator 22 and the sleep clock produced by the divider 24. The temperature signal is the digital output of the temperature sensor 4. The temperature signal is "0" while the chip temperature is not "hot". However, when the chip temperature becomes "hot", the temperature signal becomes "1", as shown at point A. The activity signal is "1" when activity is present for processing by the microprocessor 2; otherwise, the activity signal is "0" to indicate no activity is present for processing. As shown in FIG. 6, the output clock follows the fast clock only when the temperature signal is "0" and the

activity signal is "1"; otherwise, the output clock follows the sleep clock. Note that the transitions for the output clock from fast clock to sleep clock and from sleep clock to fast clock are shown as being synchronized with the low or "0" portion of the fast clock. For example, at point B the output clock would produce a partial pulse (from the fast clock) if not synchronized. Hence, it is probably preferred that switching occur only when the fast clock is "low," or when both the fast and sleep clocks are "low" as shown at point C. Note that at point C, the output clock transitions from the sleep clock to the fast clock but because the transition is synchronized with the "low" portion of the fast clock, the first pulse does not occur until point D. Such synchronization can be insured by the addition of known circuitry.

FIG. 7 is a block diagram of a fifth embodiment of the invention. Although only the clock regulation unit 20 is illustrated in FIG. 7, the fifth embodiment interacts with an oscillator 22 and a microprocessor 2 as did the third and fourth embodiments. In this embodiment, the clock regulation unit 20 includes a first divider 40 which divides the input clock (fast clock) to produce a sleep clock, and a second divider 42 which divides the input clock to produce a normal clock. The three clocks (sleep, normal and fast) are then supplied to a selector 44. The selector 44 outputs one of the three clocks as the output clock for the microprocessor 2 based on first and second select inputs IN1 and IN2. The first select input IN1 is generated by inverting the digital output from the temperature sensor 4 using an inverter 46. The second select input IN2 is generated by an activity detector 48 which functions similarly to the activity detector 12 in previous embodiments.

The activity detector 48 receives a plurality of activity inputs ACT1, ..., ACTn. For example, the activity inputs notify the activity detector 48 whether or not activity exists. Each of the activity inputs may, for example, indicate an

interrupt, keyboard activity, modem line activity, I/O port activity, or processor activity. As an example, FIG. 8 illustrates a schematic diagram of an embodiment of the activity detector 48. The activity detector 48 includes a OR gate 50 which outputs a "1" when either the activity input ACT1 or the activity input ACT2 is "1". If neither the activity signals ACT1 and ACT2 are "1", then the OR gate 50 outputs a "1", thereby indicating the presence of activity.

The following Table I illustrates the selection of one of the three clocks by the selector 44 based on the first select input IN1 and the second select input IN2.

TABLE I

IN1	IN2	CLK Mode
0	0	Sleep
0	1	Fast
1	0	Sleep
1	1	Normal

Note that when no activity is detected by the activity detector 48, then the sleep clock is output. However, when activity is detected, then the normal clock is output if the chip temperature is "hot" and the fast clock is output if the chip temperature is not "hot". Like previous embodiments, this embodiment prevents overheating and conserves energy. Many alternatives can be made to the third, fourth and fifth embodiments discussed above. For example, additional clocks with different clock frequencies could be provided and selected for different temperature ranges to provide a more gradual decrease in frequency. However, if a microprocessor has sufficient thermal heat dissipation, then even the embodiment with only two different clock frequencies (fast and sleep) may provide reasonable processing speeds even when the microprocessor is getting hot because

the switching between the clocks would be quite fast as the response of the temperature sensor 4 is very rapid because it is integrated with the microprocessor. Further, although FIGS. 4, 5, and 7 illustrate the temperature sensor 4 as resident within the clock regulation unit 20, the temperature sensor 20 need only be electrically coupled thereto and closely thermally coupled to the microprocessor 2.

FIG. 9 is a block diagram of a sixth embodiment of the invention. In this embodiment, the clock (CLK) received by a microprocessor 2 is either a sleep clock produced by an oscillator 52 or a temperature-regulated fast clock produced by a VCO 8 in accordance with a temperature signal 6 (analog) from a temperature sensor 4. Clock selection is achieved by a selector 54 based on an activity signal 14 provided by an activity detector 12, 48. The VCO 8, the temperature sensor 4 and the activity detector 12, 48 were discussed above with respect to previous embodiments. If activity is present, the temperature-regulated fast clock is supplied to the microprocessor 2. On the other hand, if no activity is detected, then the sleep clock is supplied to the microprocessor 2. The temperature regulation of the fast clock is achieved by the analog temperature signal as discussed above with regard to FIGS. 1 and 2.

Additionally, FIG. 9 illustrates an additional feature of the invention. Namely, FIG. 9 includes an analog-to-digital converter 56, a fan controller 58 and a cooling fan 60. Many conventional computing systems include a fan for circulating air through a computer's cabinet or add-on fans that provide air-flow on or near a microprocessor. Such add-on fans can be activated in accordance with ambient temperature. In contrast, the invention allows more accurate temperature monitoring of the microprocessor 2 because the temperature sensor 4 is integrated with the microprocessor 2. In addition, the invention facilitates more sophisticated energy conservation which is particularly important for portable

computing devices. The temperature signal 6 is converted to digital form by the A/D converter 56 and then supplied to the fan controller 58. The fan controller 58 performs a pulse-width modulation operation on a supply voltage (Vcc) so as to control the speed of the fan 60. Pulse-width modulation of the supply voltage allows the speed of the fan to be controlled without wasting energy. Thus, this embodiment further includes a temperature-activated, variable-speed fan.

In the case of a desk-top computing device, it is desirable to activate the fan 60 just prior to the temperature where the fast clock would be regulated downward because of high chip temperature. On the other hand, in the case of a portable computing device, it is desirable to attempt to limit the use of the fan 60 as much as possible by allowing the fast clock to be gradually reduced with increasing temperature before utilizing the fan 60. For example, if the maximum frequency of the fast clock is 100 MHz, the fan 60 could be activated in the desk-top case before the frequency would be regulated (e,g., attempts to maintain 100 MHz). This would eliminate or delay the reduction in the frequency of the fast clock. In the portable case, the fan 60 could be activated after the frequency of the fast clock is already decreased to 25 MHz. The fan 60 would then only be used when necessary to insure reasonable processing power and even then at the lowest effective, thereby saving battery energy to the extent possible.

Although not shown but described with reference to FIG. 6, depending on the particular design, synchronization of the switching of the frequency may be needed to prevent partial pulse in the clock signal. Such synchronization is easily implemented using well-known circuitry. Likewise, if the computing device requires a consistent clock period during certain events (e.g., analog-to-digital conversion), then hysteresis or other circuitry can be added to restrict the ability of the frequency of the clock to be changed during certain times.

Prior embodiments operate to decrease the clock frequency of the clock signals supplied to a microprocessor to prevent overheating and to conserve energy. FIG. 10 is a block diagram of a seventh embodiment of the invention. This embodiment operates to provide a burst processing mode for use under certain conditions. During certain types of processing activity, a clock control unit 20 causes an overdrive clock to be supplied to a microprocessor 2. Because the overdrive clock is used only in short bursts, the frequency of the overdrive clock can and preferably exceeds the frequency which sustained processing would permit without rapidly overheating.

In this embodiment, the clock control unit 20 includes a first divider 62 which divides the input clock to produce a sleep clock, and a second divider which divides the input clock to produce a fast clock. Because the input clock serves as the overdrive clock, the input clock has a clock frequency that is faster than that necessary for sufficient performance and responsiveness in most cases. The clock control unit 20 also includes a selector 66, an activity detector 68, and a temperature sensor 4. The selector 66 operates to select one of the sleep, fast or overdrive clocks based on select inputs (IN1, IN2, IN3) it receives from the activity detector 68 and the temperature sensor 4. More particularly, the activity detector 68 receives activity signals ACT1, ..., ACTn which cause the activity detector 68 to generate a burst activity signal and a normal activity signal. Certain of the activity signals ACT trigger the burst activity signal and other activity signal trigger the normal activity signal. The temperature sensor 4 is integral with the microprocessor 2 and produces a digital temperature signal which indicates whether or not the microprocessor 2 is "hot".

The following Table II illustrates the selection of one of the three clocks by the selector 66 based on the first select input IN1, the second select input IN2, and the third select input.

TABLE I

IN1	IN2	IN3	CLK Mode
0	0	0	Sleep
0	0	1	Sleep
0	1	0	Fast
0	1	1	Sleep
1	0	0	Overdrive
1	0	1	Fast/Sleep
1	1	0	Overdrive
1	1	1	Fast/Sleep

Note that when no activity (either burst or normal) is detected by the activity detector 68, then the sleep clock is output. However, when burst activity is detected, then the overdrive clock is output if the chip temperature is not "hot" and either the fast clock or the sleep clock is output if the chip temperature is "hot". The determination of which of the fast or sleep clocks to output in this situation is a design choice depending on the ability of the computing system to dissipate heat. In fact, it may be preferred to make the selection more sophisticated in this case so that selector can make the decision using addition temperature information such as signals indicating particular temperature ranges or rate at which temperature is rising. When only normal activity is detected, then the fast clock is output if the chip temperature is not "hot" and the sleep clock is output if the chip temperature is "hot". As a modification, the second divider 64 could be replaced with a VCO thereby using a temperature-regulated fast clock.

Like previous embodiments, this embodiment prevents overheating and conserves energy. The advantage of this embodiment is that processing will appear more uniform or regular to a user.

There are certain times during normal execution of a program, the computer is caused to execute operations which are beyond or unrequested by the program being executed. Such unrequested operations include interrupt processing, and data transfer to cache memory following a cache miss. Using the overdrive clock in these types of situations is advantageous because such will substantially lessen any delay induced by these unrequested operations. A computer user then perceives that the computer's responsiveness is more regular and uniform. For example, when a cache miss occurs an instruction currently being in process is not allowed to complete until the appropriate data block is loaded into the cache. The loading of the cache follow a cache miss causes the microprocessor to execute many operations for memory management that were not requested by the computer program or the user, thereby delaying the execution of the instruction. However, because the invention performs such unrequested operations at higher speeds (overdrive clock), the impact of having to perform the extra unrequested operations is substantially lessened and hopefully invisible.

In fact, a particular computer instruction could by used to indirectly select the desired clock frequency for the instruction. This could be useful for instructions that require more intensive processing than do normal instructions. An example of intensive processing is complex floating point computations. Here, the microprocessor would indicate to the activity detector that the overdrive clock is to be used if the chip temperature is not too "hot".

Yet another embodiment would be to alter processing frequency for extremely cold situations. Namely, if the temperature sensor indicates that the chip temperature (could also use ambient temperature) is less than a predetermined minimum temperature, then the clock frequency could by set regardless of activity to its maximum value to thereby cause the generation of as much heat as possible so that the computing device could operate correctly even in extremely cold

conditions. Any cooling fan of the computing device would also be shut-off using a fan controller such as shown in FIG. 9.

The many features and advantages of the present invention are apparent from the written description and thus it is intended by the appended claims to cover all such features and advantages of the invention. Further, since numerous modifications and changes will readily occur to those skilled in the art, it is not desired to limit the invention to the exact construction and operation as illustrated and described. Hence, all suitable modifications and equivalents may be resorted to as falling within the scope of the invention.

What is claimed is:

CLAIMS

1. A computer, comprising:

a clock module for producing a clock signal having two or more different frequencies;

a processor, operatively connected to said clock module, for processing instructions in accordance with the clock signal; and

a temperature sensor, operatively connected to said clock module, producing a temperature signal based on the temperature of said processor,

wherein the frequency of the clock signal supplied to said processor varies depending on the temperature of said processor.

2. A computer as recited in claim 1, wherein said processor is a microprocessor.

3. A computer as recited in claim 1, wherein said temperature sensor is thermally coupled to said processor.

4. A computer as recited in claim 1, wherein said temperature sensor is integral with the circuitry of said processor.

5. A computer as recited in claim 1, wherein said computer is a portable computing device.

6. A computer as recited in claim 1, wherein said computer further comprises:

a fan; and

a fan controller, said fan controller controls the speed of the fan in accordance with the chip temperature.

7. A clock control apparatus for a microprocessor, comprising:

a temperature sensor coupled to said microprocessor to monitor a chip temperature of the microprocessor and to produce a temperature signal in accordance with the chip temperature; and

a clock unit, operatively connected to said temperature sensor, for producing a clock for the microprocessor, the clock having a frequency dependent upon the chip temperature of the microprocessor.

8. A clock control apparatus as recited in claim 7, wherein said clock unit comprises a voltage-controlled oscillator (VCO), said VCO receives a chip temperature signal from said temperature sensor and produces the clock having a frequency dependent upon the chip temperature.

9. A clock control apparatus as recited in claim 7,

wherein said clock control apparatus further comprises an activity detector for detecting activity by the microprocessor and producing an activity signal in accordance therewith, and

wherein said clock unit comprises:

a VCO controller for producing a control signal based on the activity signal from said activity detector and a chip temperature signal from said temperature sensor; and

a voltage-controlled oscillator, said voltage-controlled oscillator produces the clock having a frequency dependent upon the control signal.

10. A clock control apparatus as recited in claim 7, wherein said temperature sensor and said clock unit are integral with said microprocessor,

wherein said clock control apparatus further comprises detection means for monitoring activity of the microprocessor, and

wherein the clock produced by said clock unit has its frequency dependent upon both the activity and the chip temperature.

11. A method for producing a clock for a microprocessor,

(a) monitoring chip temperature of the microprocessor;

(b) producing a clock signal having a frequency which varies in accordance with the chip temperature; and

(c) supplying the clock signal to the microprocessor.

12. A method as recited in claim 11, wherein the frequency is altered in real-time as the chip temperature changes, and

wherein the frequency of the clock signal decreases gradually as the chip temperature increases beyond a predetermined chip temperature.

13. A method as recited in claim 11, wherein said producing (b) comprises:

(b1) receiving a slow frequency clock and a fast frequency clock; and

(b2) selecting the slow frequency clock if the chip temperature exceeds a predetermined temperature, otherwise selecting the fast frequency clock.

14. A method as recited in claim 11,

wherein said method further comprises (d) monitoring activity of the microprocessor, and

wherein said producing (b) comprises:

(b1) receiving a slow frequency clock and a fast frequency clock; and

(b2) selecting the slow frequency clock if the chip temperature exceeds a predetermined temperature or if there is no activity at the microprocessor, otherwise selecting the fast frequency clock.

15. A method as recited in claim 11,

wherein said method further comprises (d) monitoring activity of the microprocessor, and

wherein said producing (b) comprises:

(b1) receiving a plurality of clocks, each clock having a different frequency; and

(b2) selecting one of the clocks based on the chip temperature and the activity of the microprocessor.

16. A method as recited in claim 15, wherein one of the clocks is an overdrive clock, and

wherein the overdrive clock is selected when certain activity is present and the chip temperature is below a predetermined temperature.

17. A method as recited in claim 16, wherein when the certain activity is completed the overdrive clock is replaced by one of the other clocks.

18. A method as recited in claim 11, wherein said producing (b) comprises (b1) producing a variable-frequency clock, the frequency of the variable-frequency clock being varied in accordance with the chip temperature.

19. A method as recited in claim 18,

wherein said method further comprises (d) monitoring activity of the microprocessor, and

wherein said producing step (b) further comprises:

(b2) receiving a fixed-frequency clock; and

(b3) selecting one of the variable-frequency clock and the fixed-frequency clock based on the activity of the microprocessor.

20. A method as recited in claim 11, wherein said method further comprises (d) producing a variable-speed control signal for a fan with the speed being dependent on the chip temperature.

ABSTRACT

Novel techniques for controlling a processor's clock frequency so as to prevent overheating are disclosed. The invention attempts to maximizes the processing speed of the processor while preventing overheating. In a preferred embodiment, the invention monitors a processor's activity and its temperature. When there is no activity for the processor, a slowed clock frequency is used, thereby saving power and lowering the thermal heat produced by the processor. On the other hand, when there is activity for the processor, a fast clock frequency is used. However, when prolonged activity (i.e., sustained fast clock frequency) causes the processor's temperature to become dangerously high for proper operation, the clock frequency is reduced so as to maintain processing speed at a reduced speed while preventing overheating. The invention may be implemented as an apparatus or a method.

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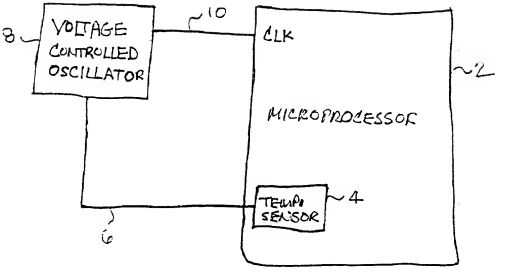

FIG. 1

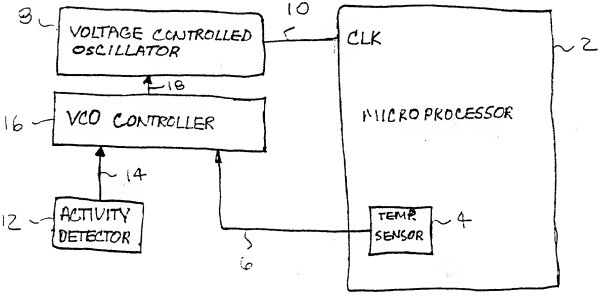

FIG. 3

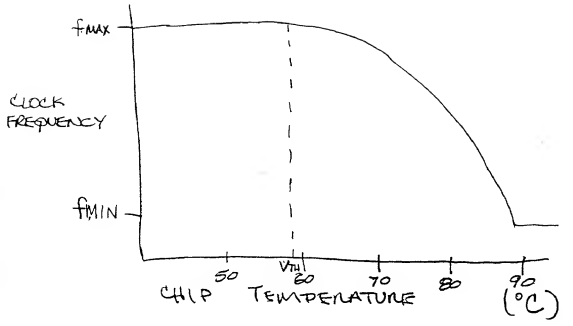

FIG. 2

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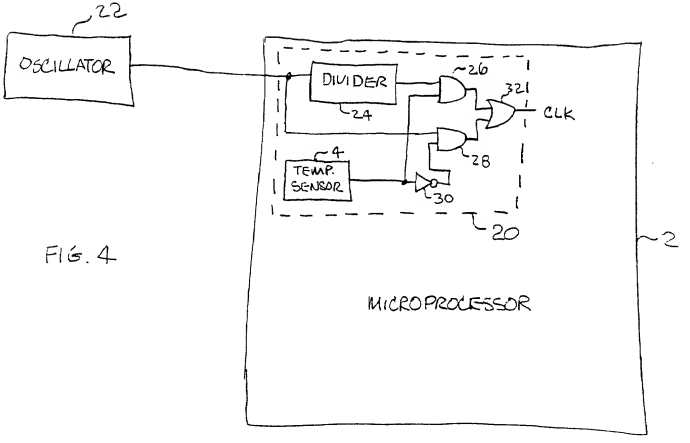


FIG. 4

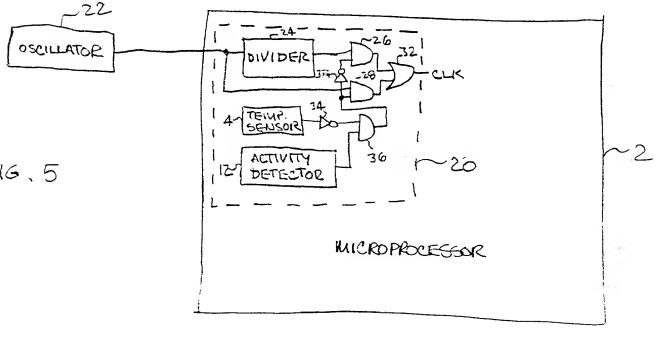
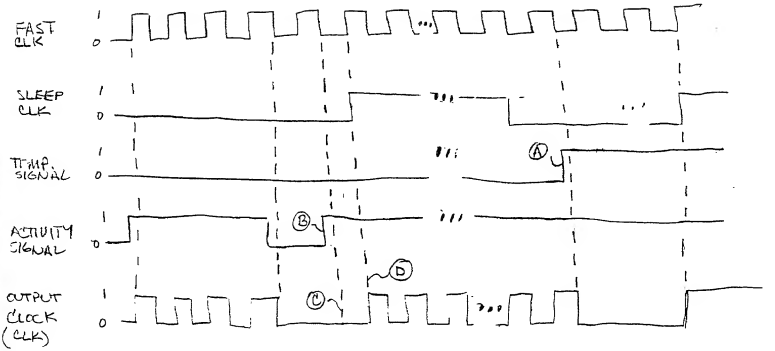


FIG. 5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SLEEP CLK
TEMP. SIGNAL
ACTIVITY SIGNAL
OUTPUT CLOCK (CLK)
1
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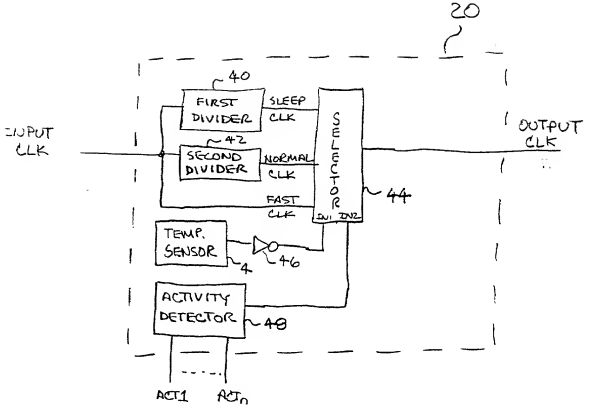
A
B
C
D

FIG. 6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40
FIRST DIVIDER
SLEEP CLK
42
SECOND DIVIDER
NORMAL CLK
FAST CLK
SELECTOR
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44
INPUT CLK
OUTPUT CLK
TEMP. SENSOR
46
ACTIVITY DETECTOR
48
ACT1
ACTn

FIG. 7

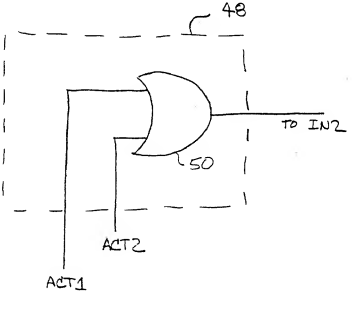
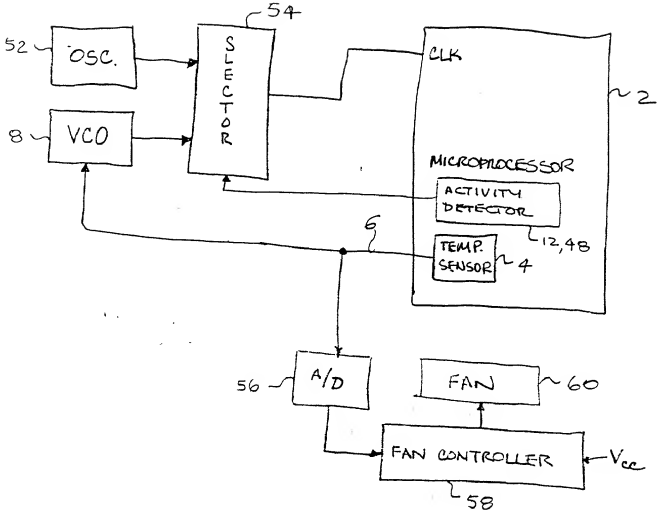

48
TO IN2
50
ACT2
ACT1

FIG. 8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52
OSC.
SELECTOR
CLK
2
8
VCO
MICROPROCESSOR
ACTIVITY DETECTOR
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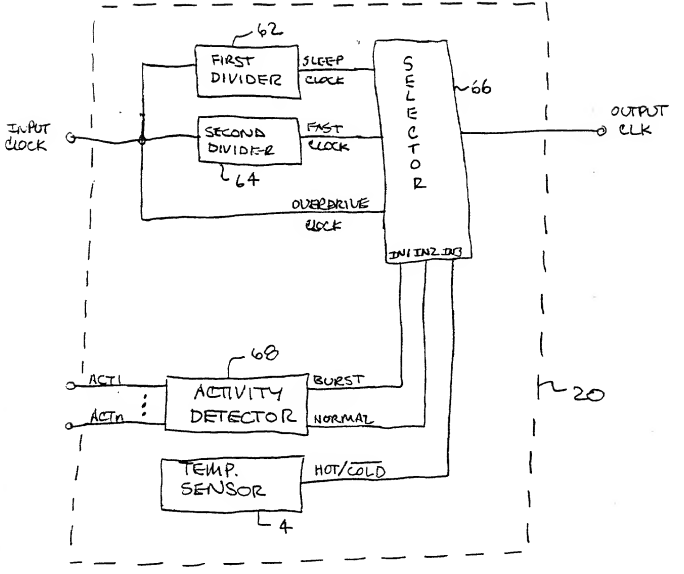
6
TEMP. SENSOR
4
56
A/D
FAN
60
FAN CONTROLLER
V_{cc}
58

FIG. 9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SLEEP CLOCK
SELECTOR
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INPUT CLOCK
SECOND DIVIDER
FAST CLOCK
OUTPUT CLK
64
OVERDRIVE CLOCK
IN1 IN2 IN3
68
ACT1
ACTn
ACTIVITY DETECTOR
BURST
NORMAL
20
TEMP. SENSOR
HOT/COLD
4

FIG. 10

SOLE/JOINT

I LARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name: that I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural names are listed below) of the subject matter claimed and for which a patent is sought in the application entitled:

METHOD AND APPARATUS FOR CONTROLLING A PROCESSOR'S CLOCK FREQUENCY IN ACCORDANCE WITH THE PROCESSOR'S TEMPERATURE

which application is:
__X__ the attached application (for original application)
_____ application Serial No. _____, filed _____, and amended on _____ (for declaration not accompanying application)

that I have reviewed and understand the contents of the specification of the above-identified application, including the claims, as amended by an amendment referred to above; that I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application under 37 C.F.R. 1.56(a), that I hereby claim foreign priority benefits under Title 35, United States Code §119, §172 or §365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified on said list any foreign application for patent or inventor's certificate on this invention having a filing date before that of the application on which priority is claimed:

Application Number	Country	Filing Date	Priority Claimed
			☐ (yes or no)
			☐
			☐

I hereby claim the benefit of Title 35, United States Code §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in a listed prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge my duty to disclose any material information under 37 C.F.R. 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status (patented, pending, abandoned)

I hereby appoint C. Douglass Thomas, Reg. No. 32,947 my attorney to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and request that all correspondence about the application be addressed to C. Douglass Thomas, 1193 Capri Drive, Campbell, CA 95008.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date 6/11/97 First Inventor C. Douglass Thomas
(First Name / Middle Initial / Last Name)
Residence Campbell, CA Signature C. Douglass Thomas
Post Office Address 1193 Capri Drive
Citizenship USA Campbell, CA 95008

Date 6/5/97 Second Inventor Alan E. Thomas
(First Name / Middle Initial / Last Name)
Residence Ocean City, NJ Signature Alan E. Thomas
Post Office Address 424 Atlantic Avenue
Citizenship USA Ocean City, NJ 08226

In the United States Patent and Trademark Office

First/Sole Applicant: C. DOUGLASS THOMAS

Joint/Second Applicant: ALAN E. THOMAS

Title: "METHOD AND SYSTEM FOR CONTROLLING A PROCESSOR'S CLOCK FREQUENCY IN ACCORDANCE WITH THE PROCESSOR'S TEMPERATURE"

Small Entity Declaration—Independent Inventor(s)

As a below-named inventor, I hereby declare that I qualify as an independent inventor as defined in 37 CFR 1.9(c) for purposes of paying reduced fees under Section 41(a) and (b) of Title 35 United States Code, to the Patent and Trademark Office with regard to my above-identified invention described in the specification filed herewith. I have not assigned, granted, conveyed, or licensed—and am under no obligation under any contract or law to assign, grant, convey, or license—any rights in the invention to either (a) any person who could not be classified as an independent inventor under 37 CFR 1.9(c) if that person had made the invention, or (b) any concern which would not qualify as either (i) a small business concern under 37 CFR 1.9(d) or (ii) a nonprofit organization under 37 CFR 1.9(e).

Each person, concern, or organization to which I have assigned, granted, conveyed, or licensed—or am under an obligation under contract or law to assign, grant, convey, or license—any rights in the invention is listed below:

☒ There is no such person, concern, or organization.

☐ Any applicable person, concern, or organization is listed below:*

Full Name: _____

Address: _____

_____

I acknowledge a duty to file, in the above application for patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b)).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

C. Douglass Thomas
Signature of Sole/First Inventor

C. DOUGLASS THOMAS
Print Name of Sole/First Inventor

Date of Signature: 6/12/94

Alan E. Thomas
Signature of Joint/Second Inventor

ALAN E. THOMAS
Print Name of Second/Joint Inventor

Date of Signature: 6/15/94

*Note: A separate Small Entity Statement is required from any listed entity.

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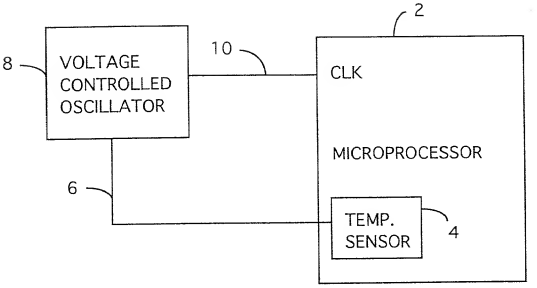

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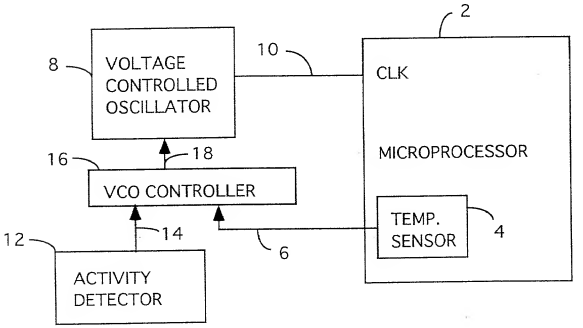

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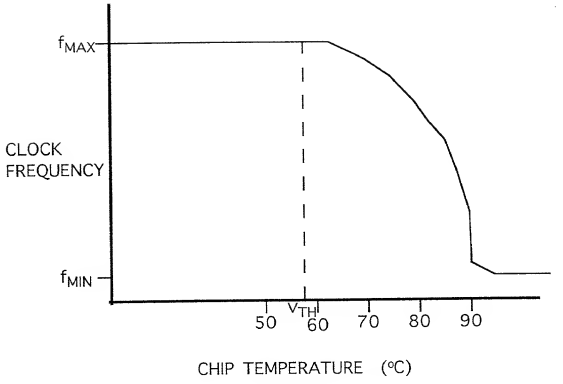

FIG. 2

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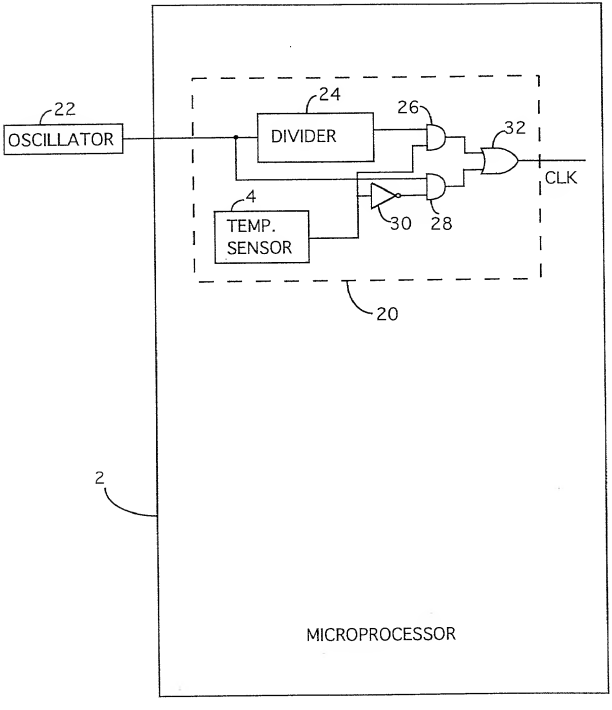

FIG. 4

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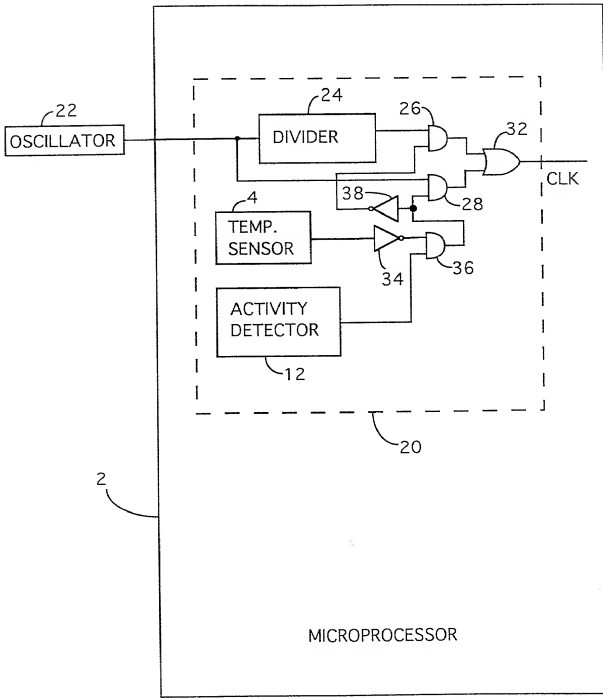

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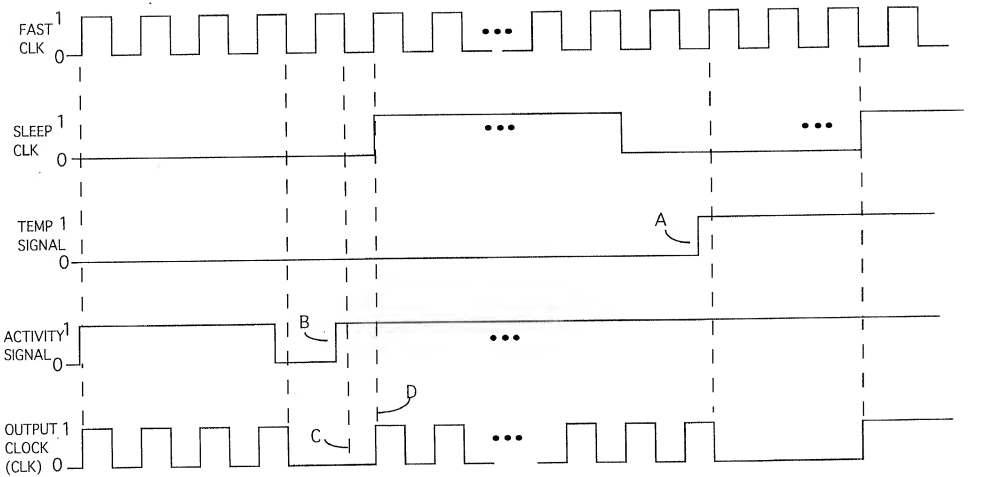

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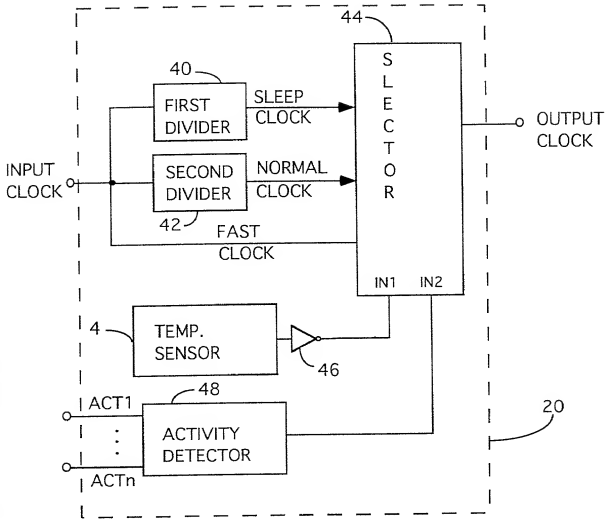
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40
FIRST DIVIDER
SLEEP CLOCK
SECOND DIVIDER
NORMAL CLOCK
42
FAST CLOCK
SELECTOR
IN1
IN2
OUTPUT CLOCK
INPUT CLOCK
4
TEMP. SENSOR
46
48
ACT1
ACTn
ACTIVITY DETECTOR
20

FIG. 7

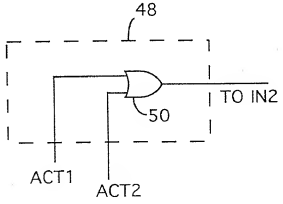
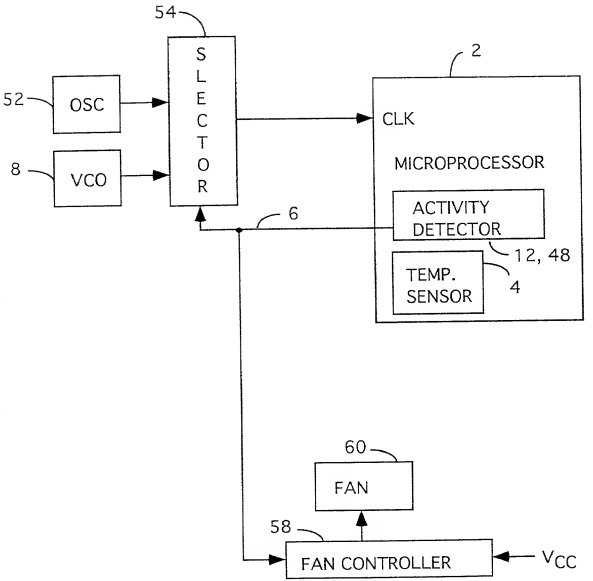

48
TO IN2
50
ACT1
ACT2

FIG. 8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SELECTOR
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OSC
8
VCO
2
CLK
MICROPROCESSOR
ACTIVITY DETECTOR
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6
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FAN
58
FAN CONTROLLER
V_{CC}

FIG. 9

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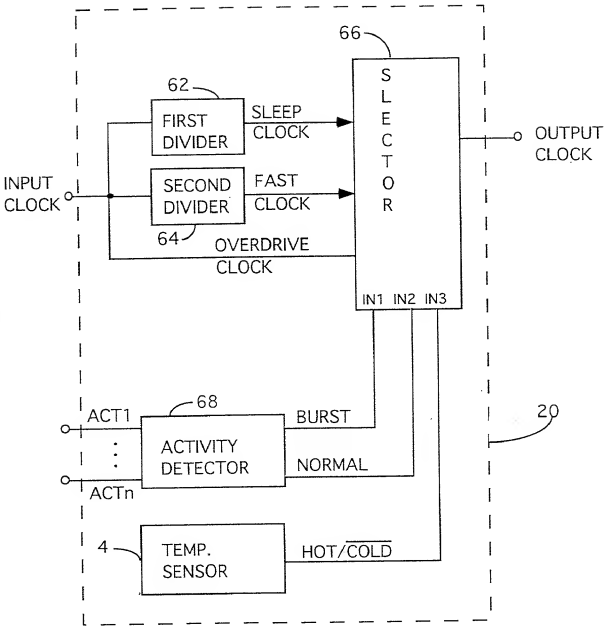

FIG. 10